AMENDMENTS TO THE CLAIMS

The following listing of claims will replace all prior versions and listings of claims in the application.

LISTING OF THE CLAIMS

The following listing of claims will replace all prior versions and listings of claims in the application.

1. (Currently Amended) An integrated burn-in test method for testing a multi-chip package, comprising:

uploading an integrated burn-in test program to burn-in equipment for testing the multi-chip package having multiple kinds of semiconductor devices; and

conducting a test on each of the multiple kinds of semiconductor devices using the integrated burn-in test program; wherein,

the multiple kinds of semiconductor devices include at least ~~one~~ two of a non-volatile memory, a SRAM, and a DRAM, and the integrated burn-in test program is adapted to test ~~at least one of~~ the non-volatile memory, the SRAM, and the DRAM.

2. (Canceled)

3. (Canceled)

4. (Original) The method of claim 1, wherein the multi-chip package performs a memory function.

5. (Previously Presented) The method of claim 1, wherein the test is conducted for each of the semiconductor devices at a different temperature.

6. (Previously Presented) The method of claim 1, wherein the multi-chip package is loaded on a burn-in board and the burn-in board is loaded in a chamber of burn-in equipment.

7. (Original) The method of claim 1, wherein the multi-chip package is in the form of a TBGA (thin ball grid array).

8. (Previously Presented) The method of claim 1, wherein the integrated burn-in test program uses a multiplexer selection function for applying a desired test condition during testing of each of the semiconductor devices.

9. (Original) The method of claim 1, wherein the integrated burn-in test program has an I/O masking function for blocking some I/O terminals.

10. (Previously Presented) The method of claim 1, wherein the integrated burn-in test program has a function of setting a burn-in temperature condition for each of the semiconductor devices.

11. (Previously Presented) The method of claim 6, wherein after loading the multi-chip package on the burn-in board to the chamber of the burn-in equipment, a contact test is conducted to examine whether an electrical connection of the burn-in board is correct.

12. (Original) The method claimed in claim 1, wherein the burn-in test is a monitoring burn-in test.

13. (Original) The method of claim 1, wherein the integrated burn-in test program requires only one time bin sorting based on the burn-in test result.

14. (Currently Amended) An integrated burn-in test method for testing a multi-chip package, comprising:

uploading an integrated burn-in test program to test the multi-chip package having multiple kinds of semiconductor devices to burn-in equipment, the multiple kinds of semiconductor devices include at least two of a non-volatile memory, a SRAM, and a DRAM;

conducting a contact test for a burn-in board to examine an electrical connection;

conducting a burn-in test for each of the semiconductor devices using a multiplex selection function of the integrated burn-in test program loaded to the burn-in equipment, the burn-in test for each of the semiconductor devices is performed sequentially and the integrated burn-in test program controls the chamber temperature according to a test temperature for each of the semiconductor devices;

ending the burn-in test; and

bin sorting the multi-chip package based on the burn-in test result.

15. (Canceled)

16. (Previously Presented) The method of claim 14, wherein each of the semiconductor devices performs a memory function.

17. (Original) The method of claim 14, wherein the integrated burn-in test program has an I/O masking function for blocking some I/O terminals.

18. (Original) The method of claim 17, wherein each semiconductor device of the multi-chip package has a different number of I/O terminal pins.

19. (Original) The method of claim 14, wherein the multi-chip package is in the form of a TBGA (thin ball grid array).

20. (Original) The method of claim 14, wherein the burn-in test is a monitoring burn-in test.

21. (Currently Amended) An integrated burn-in test method for testing a multi-chip package, comprising:

providing the multi-chip package formed of multiple kinds of semiconductor devices; and

testing the multi-chip package with an integrated burn-in test program, wherein the burn-in test program is adapted to test each of the semiconductor devices; wherein,

the multiple kinds of semiconductor devices include at least ~~one~~ two of a non-volatile memory, a SRAM, and a DRAM, and the integrated burn-in test program is adapted to test ~~at least one of~~ the non-volatile memory, the SRAM, and the DRAM.

22. (Previously Presented) The method of claim 21, wherein the testing includes applying a specific test condition during testing of each of the semiconductor devices, wherein the specific test condition is defined by a multiplexer selection function.

23. (Original) The method of claim 21, wherein the testing includes blocking some I/O terminals during testing of some semiconductor devices, wherein the blocking is defined by an I/O masking function.

24. (Previously Presented) The method of claim 21, wherein the testing includes setting a specific burn-in temperature condition for each of the semiconductor device~~s~~.

25. (Previously Presented) The method of claim 21, wherein the testing includes performing a single contact test.

26. (Previously Presented) The method of claim 21, further comprising:

a one time bin sorting for the multi-chip package based on the testing result.

27. (Currently Amended) An integrated burn-in test method for testing a multi-chip package, comprising:

providing the multi-chip package formed of multiple kinds of semiconductor devices, the multiple kinds of semiconductor devices include at least two of a non-volatile memory, a SRAM, and a DRAM;

testing the multi-chip package with an integrated burn-in test program adapted to test each of the semiconductor devices, including

performing a single contact test for each of the semiconductor device,

blocking some I/O terminals during testing of some semiconductor devices, wherein the blocking is defined by an I/O masking function,

setting a specific burn-in temperature condition for each of the semiconductor devices,

conducting a burn-in test for the multi-chip package by applying a specific test condition for each of the semiconductor devices, wherein the specific test condition is defined by a multiplexer selection function; and

a one time bin sorting of the multi-chip package based on the testing result.

28. (Previously Presented) The method of claim 1, further comprising:

loading the multi-chip package to a chamber of the burn-in equipment.

29. (Previously Presented) The method of claim 14, further comprising:

loading the multi chip-package on the burn-in board; and

loading the burn-in board into a chamber of the burn-in equipment.

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